USN | | | | | | | | | | |

12EC021

M.Tech. Degree Examination, June/July 2013
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. With suitable equations, describe the secondary effects associated with a MOS transistor operation. **(12 Marks)**

b. Briefly explain i) Static load MOS inverters ii) Tristate inverter. **(08 Marks)**

2 a. Show how the NMOS inverter and CMOS inverter delay is estimated. **(06 Marks)**

b. Explain lambda based rules and their significance. **(08 Marks)**

c. Describe metal interconnected and polysilicon/refractory metal interconnect associated with CMOS process enhancement. **(06 Marks)**

3 a. Obtain the scaling factors for the following :
i) Gate area. ii) Switching energy/gate iii) Channel resistance. **(06 Marks)**

b. Draw the CMOS circuit and stick diagram for the function $\overline{A \oplus B}$. **(06 Marks)**

c. With relevant response curves, explain the transmission gate output characteristics for change in control input and for change in switched input. **(08 Marks)**

4 a. With a neat diagram, explain CMOS 2 input NOR gate and specify the condition for Kn and Kp to get $V_{th} = \frac{V_{DD}}{2}$. **(08 Marks)**

b. Explain the function of D latch with gate level schematic and CMOS circuit. **(06 Marks)**

c. Write a note on latch up in CMOS. **(06 Marks)**

5 a. Dynamic CMOS logic circuit cannot be cascaded. Justify the statement. **(06 Marks)**

b. What is voltage boot strapping? Explain. **(08 Marks)**

c. Describe pass transistor logic in brief. **(06 Marks)**

6 a. Explain the salient aspects of differential amplifier and derive the expression for its gain. **(08 Marks)**

b. Briefly explain current mirrors. **(07 Marks)**

c. Explain CMOS/SOS technology. **(05 Marks)**

7 a. Briefly explain the clock distribution network with relevant sketches. **(05 Marks)**

b. Describe charge storage and charge leakage problems in a clocked circuit and their amplitudes. **(08 Marks)**

c. Briefly explain NORA CMOS logic (NP-donino logic). **(07 Marks)**

8 Write short notes on:

a. Pass transistor circuits.

b. Scaling of MOS circuits.

c. Noise margin.

d. Band gap references. **(20 Marks)**

* * * * *